NO. 1

QUARTERLY REPORT

FOR

ANALOG-TO-DIGITAL CONVERTER

Contract No. N00014-87-C-0314

30 March 1987 - 30 June 1987

ARPA Order Number:	9117
Program Code Number:	
Name of Contractor:	Texas Instruments Incorporated 13500 N. Central Expressway P. O. Box 655936, M. S. 105 Dallas, Texas 75265
Effective Date of Contract:	30 March 1987
Contract Expiration Date:	28 February 1990
Contract Number:	N00014-87-C-0314
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Program Manager:	Bill Wisseman (214) 995-2451
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Short Title of Work:	GaAs A-to-D Converter
Contract Period Covered by Report:	30 March 1987 - 30 June 1987

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I. SUMMARY

A. Brief Program Definition

This is a research and development program to design and fabricate both a GaAs high sampling rate A/D converter and a high resolution GaAs A/D converter.

B. Process Development Test Chip

A new process development test chip has been designed and reticles have been received. This test chip is designed to isolate the critical factors that impact the GaAs HBT dc parameters such as gain, leakage currents, and breakdown voltages. This mask set will be used for both our baseline nonself-aligned HBT process and for the development of the advanced self-aligned HBT process.

C. AlGaAs/GaAs Material

A good working relationship has been established with VARO, Inc. for obtaining specific MOCVD AlGaAs/GaAs epitaxial films with various layer thicknesses, dopings, and bandgap gradings. Four lots of material have been obtained for evaluation and seven additional lots have been ordered.

II. HETEROJUNCTION BIPOLAR PROCESS DEVELOPMENT

The ADC circuit design requires that the transistor emitters be isolated, which requires that the transistors be fabricated with the emitters on the top surface. To make these emitter-up transistors compatible with VLSI, it is necessary to develop a bipolar process that does not rely on mesa etching for isolation and/or connections to the various transistor layers.

The initial task required for the successful completion of this contract is to optimize the characteristics of our emitter-up bipolar transistors. In particular, the transistor gains at low current and small emitter sizes must be improved along with a needed reduction in the contact resistances for nonalloyed contacts. Toward these ends, a mask set was generated to address the various process trade-offs.

A. New Process Development Test Chip

Effort during the first quarter of this program was primarily directed toward a test chip design and layout. The design has been completed and a mask set has been received. Figure 1 shows the layout of the new test chip. It is designed with a series of submodules. The bonding pad layout for each submodule is the same, permitting most of the electrical structures to be automatically probed.

The design encompasses both nonself-aligned and self-aligned transistor processes. Table 1 gives an overview of the test structures that are aimed at isolating the critical factors impacting the transistor dc parameters such as gain, leakage currents, and breakdown voltages. In addition to the transistors, there are both process and device evaluation test structures included in this design. Large area capacitors have been designed to extract the various transistor and interconnect capacitances. Kelvin sheet resistance structures have been designed for both process control and device evaluation. Various stitch patterns and large transistors have been designed for in-process go/no go tests.

Table 2 lists the various HBT transistors that have been designed, along with a summary of their critical geometries. The transistor dimensions listed in Table 2 are illustrated in Figure 2. Bipolar transistors with emitter sizes varying from 2 x 2 μm to 250 x 250 μm have been designed for evaluating the impact of the size and periphery on the transistor dc parameters. In addition, the proximity of the boron damage isolation implant with respect to the base-emitter junction will also be evaluated. The impact of various spacings will be evaluated using multiple transistors designed with essentially the same dimensions except for the key dimension being evaluated.

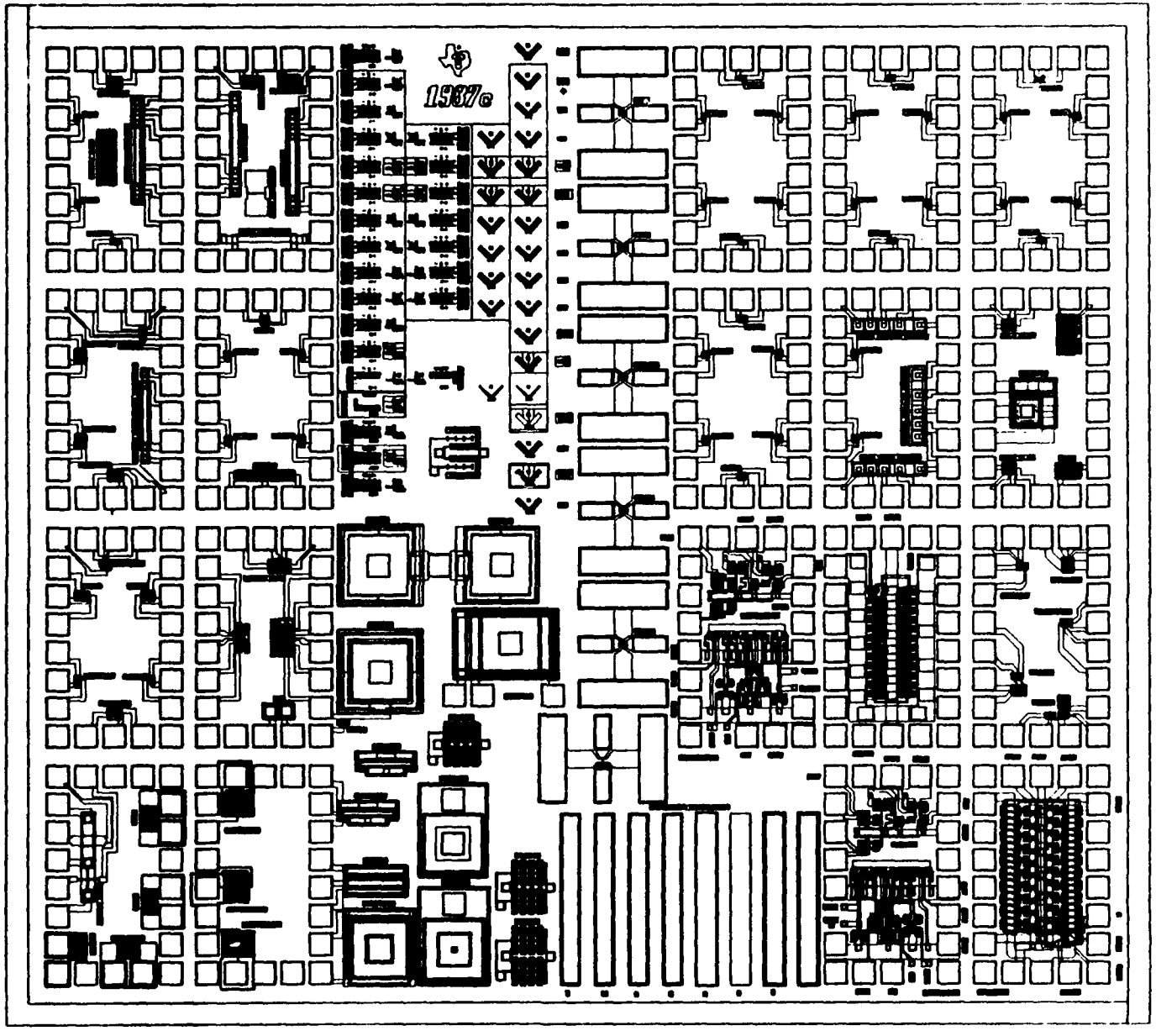


Figure 1. ADC process development test chip.

Table 1. ADC Test Bar Functions

Function	Nonself Align	Self Align
Gain (Bipolar) Size Effects Boron Damage Guard Ring	 3 x 3 μm^2 to 250 x 250 μm^2 6, 2, 1 μm space or overlap Be Multiple structures	 2 x 2 μm^2 - 25 x 250 μm^2 1, 2, 3 μm space None
Process Monitors	All implants R_S, C-V, Kelvin spreading resistance	Same
In-Process Test	Large transistors and stitch patterns	Same
Yield Go/No Go	Stitch patterns, metal continuity, intralevel shorts	Same
Trench	Metal continuity, SEM monitors	Same
Circuits	Op amp, comparator, R.O. (7 x 7 emitters)	None
Load Resistors	Stitch pattern, sheet, in-process etch test	Same
S-parameters	4 HBT Arrays	1 HBT Array
JFETs	W/L 8 μm/5 μm to 250 μm/250 μm	Same
Schottky Diodes	3 x 7 μm^2 to 250 x 250 μm^2	Same

Table 2. Summary of Transistor Designs and Critical Geometries
(All dimension in μm)

A. Nonself-Aligned Process

Test Structure	Emitter A x B	Base C x D	Outer p^+ E x F	$n^+ - p^+$ Space G	n^+ Collector H x I	Emitter to Boron K	Boron Block M x N
E3x3	3 x 3	7 x 7	14 x 9	3	4 x 8	2	12.5 x 7
E5x5	5 x 5	9 x 9	17 x 11	3	5 x 11	2	15 x 9
E5x5-2	5 x 5	15 x 15	16 x 16	3	8 x 14		
E7x7	7 x 7	11 x 11	19 x 13	3	7 x 14	2	19.5 x 11
E7x7-2	7 x 7	11 x 11	19 x 17	3	7 x 17	2	17 x 15
E7x21	7 x 21	11 x 25	21 x 27	3	7 x 27	2	19.5 x 25
E7x42	7 x 42	11 x 46	21 x 48	3	7 x 48	2	19.5 x 46
E9x50	9 x 50	13 x 54	23 x 56	3	7 x 56	2	21.5 x 54
E9x254	9 x 254	13 x 258	23 x 260	3	7 x 260	2	21.5 x 258
E11x11	11 x 11	15 x 15	25 x 17	3	7 x 17	2	23.5 x 15
E14x14	14 x 14	18 x 18	28 x 20	3	7 x 20	2	25.5 x 18
E25x25-1	25 x 25			3			
E25x25-2	25 x 25			3			
E25x25-3	25 x 25			3			
E25x25-4	25 x 25			3			
E25x25-5	25 x 25			3			
E25x250	25 x 250	33 x 258	43 x 262	4	29 x 262		5
E250x250	250 x 250	260 x 260	294 x 274	4	-		13

Table 2. (Continued)

B. Self-Aligned Process

Test Structure	Emitter A x B	Base C x D	Outer p^+ E x F	$n^+ - p^+$ Space G	n^+ Collector H x I	Emitter to Boron K	Boron Block M x N
1A-1	2 x 2	6 x 6	15 x 8	1	8 x 8	1	10 x 15
1A-2	2 x 2	6 x 6	16 x 8	1	8 x 8	2	12 x 7
1B-1	5 x 5	9 x 9	18 x 11	1	8 x 11	1	13 x 7
1B-2	3 x 5	7 x 9	18 x 11	2	8 x 11	1	12 x 7
1B-3	3 x 5	7 x 9	18 x 11	1	8 x 11	1	13 x 7
1B-4	3 x 5	7 x 9	16 x 11	3	8 x 11	1	11 x 7
1B-5	5 x 3	9 x 9	18 x 11	1	8 x 11	1	13 x 7
1C-1	5 x 5	9 x 9	22 x 11	3	8 x 17	1	17 x 7
1C-2	5 x 5	9 x 9	25 x 13	1	8 x 17	1	17 x 7
1C-3	5 x 5	9 x 9	25 x 13	1	8 x 17	2	19 x 9
1C-4	9 x 9	13 x 13	22 x 15	3	8 x 17	1	17 x 11
1C-5	9 x 13	13 x 17	22 x 19	1	8 x 17	1	17 x 15
1C-6	3 x 13	13 x 17	22 x 19	1	8 x 17	1	17 x 15
1-OPT	25 x 250	45 x 270	85 x 280	5	45 x 270	5	60 x 260

Table 2. (Continued)

Self-Aligned Process (Continued)

Test Structure	Emitter A x B	Base C x D	Outer p^+ E x F	$n^+ - p^+$ Space G	n^+ Collector H x I	Emitter to Boron K	Boron Block M x N
3A-1	2 x 2	6 x 6	15 x 20	1	8 x 20	1	10 x 16
3A-2	2 x 2	6 x 6	16 x 20	0	8 x 20	2	11 x 16
3A-3	2 x 2	6 x 6	16 x 20	1	8 x 20	2	11 x 16
3B-1	2 x 2	6 x 6	15 x 26	1	8 x 26	1	10 x 22
3B-2	2 x 4	6 x 8	15 x 26	1	8 x 26	1	10 x 22
3B-3	2 x 6	6 x 10	15 x 26	1	8 x 26	1	10 x 22
3B-4	2 x 8	6 x 12	15 x 26	1	8 x 26	1	10 x 22

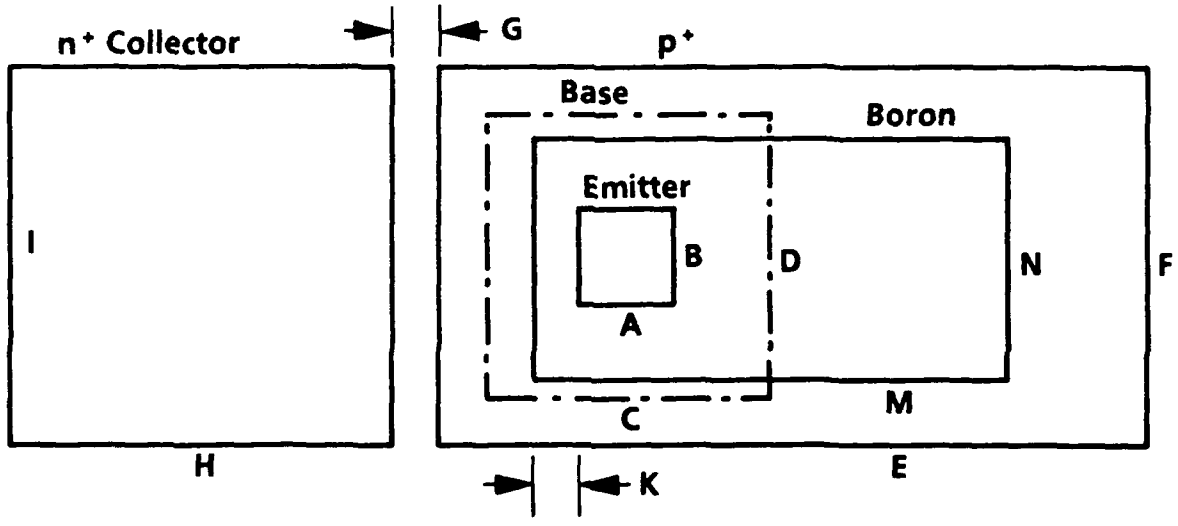


Figure 2. Transistor layout.

Several of the various HBT transistor layouts were designed with interconnects compatible with the use of the Cascade Microtech microwave wafer probe for high frequency S-parameter evaluations and f_t measurements. These can be seen in the center of Figure 1. In addition to the cascade connections for the transistors, a 50-ohm termination and an open circuit have been connected with cascade connections for calibrating the measurement system.

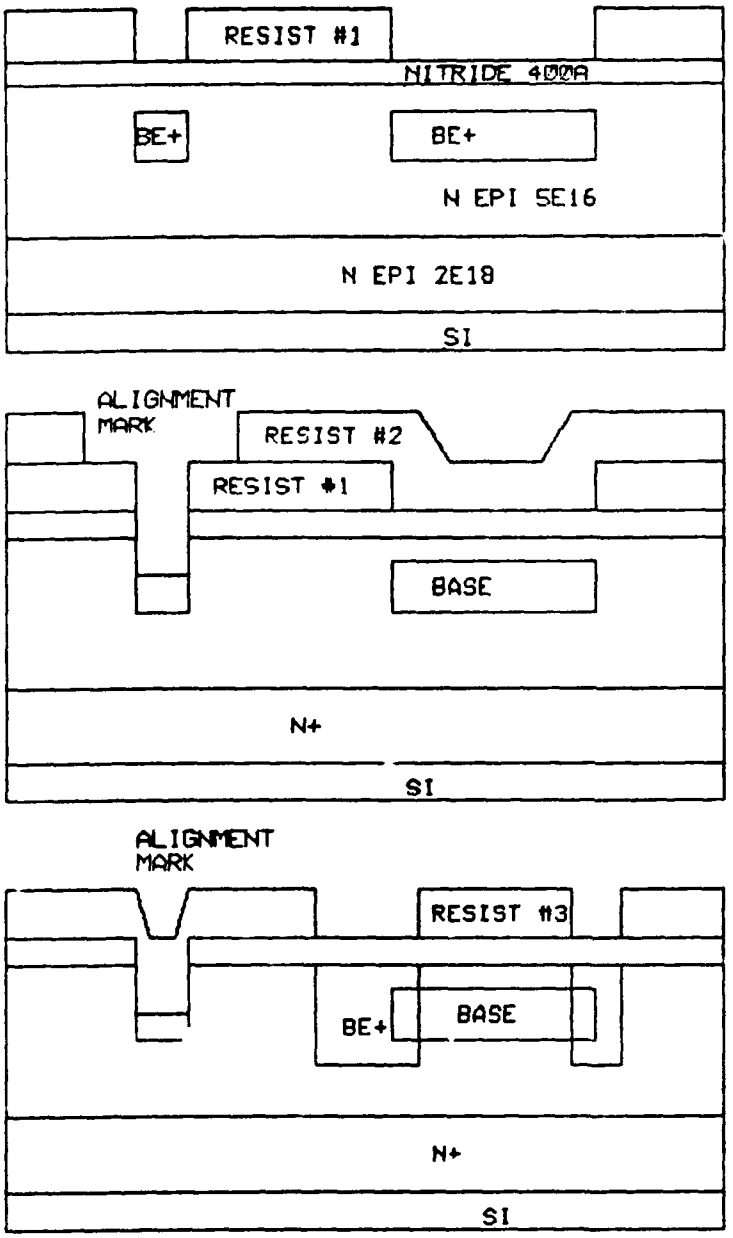
Schottky diodes and JFETs, which will be fabricated with the HBT process, have been designed with various layouts to evaluate these devices electrically.

There are several simple circuits designed on the test chip that include an ECL ring oscillator, a STL ring oscillator, two op-amps, and two comparator circuits. One of the comparator circuits is fabricated using nonself-aligned transistors, while the second was designed with self-aligned transistors. The remainder of the above circuits are designed with nonself-aligned transistors.

B. Baseline Process

The baseline process to be developed during the first six months of the contract will be a planar nonself-aligned process in which the transistor base is implanted below the AlGaAs interface and trench isolation will be used for transistor-transistor isolation. This process is schematically illustrated in Figures 3(a) through 3(c). The maximum base concentration in this process must be less than the emitter doping to prevent the type conversion of the AlGaAs emitter. This will put a lower limit on the base resistance, which will impact its frequency response.

Although this baseline process is expected to be used for the initial circuit evaluations, it is not expected to meet the maximum frequency requirements of the ADC. Toward that end, advanced processes will be developed. These advanced processes will proceed along two parallel paths. First, the "overgrowth" process will address methods for lowering the base sheet resistance and reducing the base width to lower the transit time and

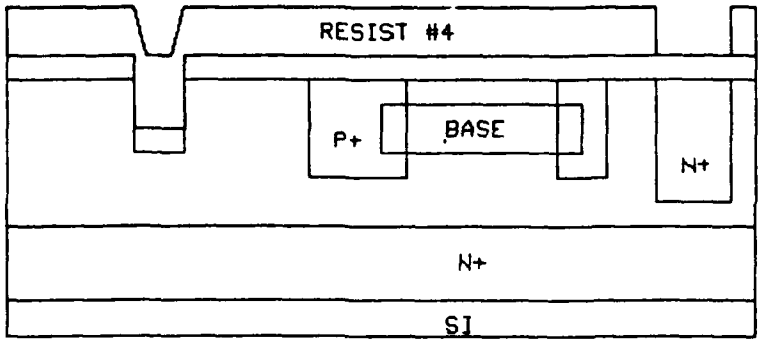


DEPOSIT 400A° NITRIDE
PATTERN BASE
IMPLANT BE+

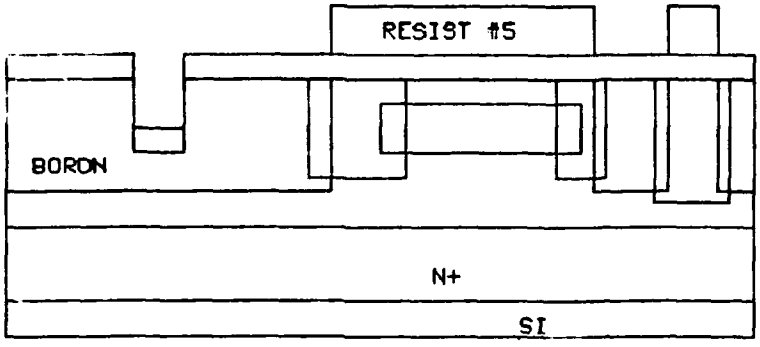
SECOND COAT RESIST
PATTERN ALIGNMENT MARKS
PLASMA ETCH NITRIDE
WET ETCH GAAS
STRIP RESIST

PATTERN P+ RESIST
IMPLANT BE+
STRIP RESIST

Figure 3(a). ADC nonself-aligned process.

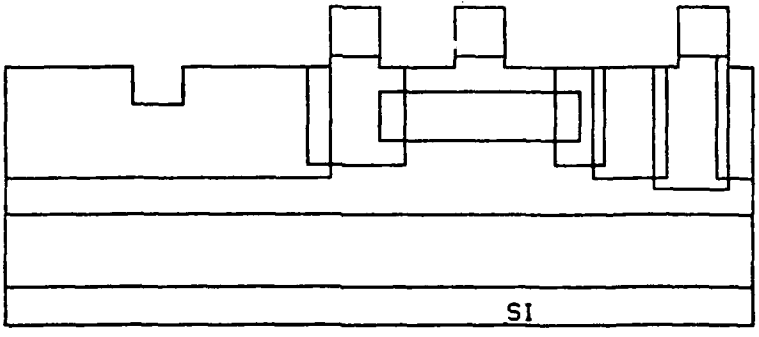


PATTERN N+ RESIST
IMPLANT SI+
STRIP RESIST
RAPID THERMAL ANNEAL



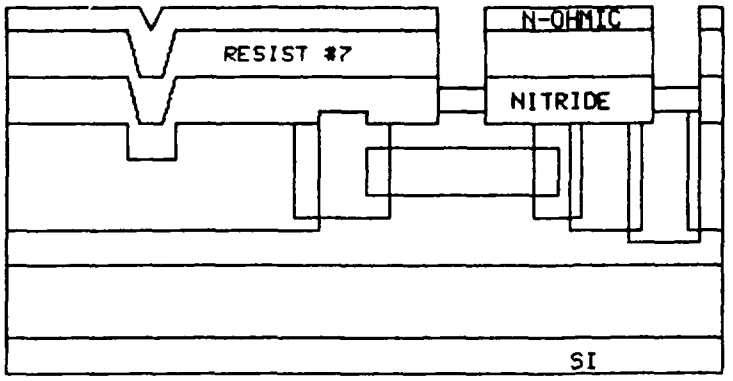
PATTERN ISOLATION RESIST
IMPLANT BORON
STRIP RESIST
STRIP NITRIDE

RESIST #6

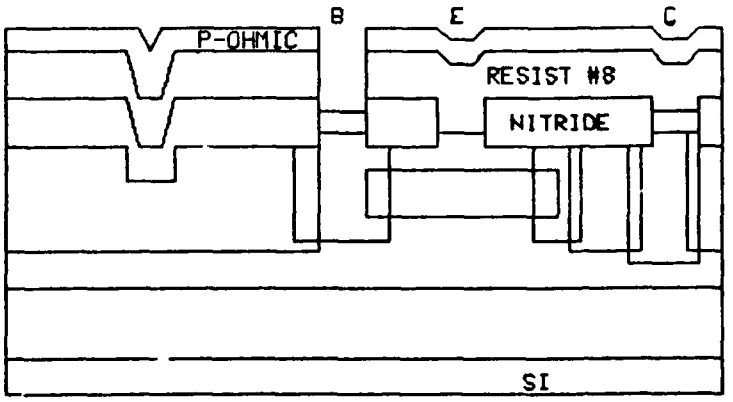


PATTERN RESIST
FOR CAP ETCH
REMOVE N+ GAAS
CAP LAYER WET ETCH
STRIP RESIST

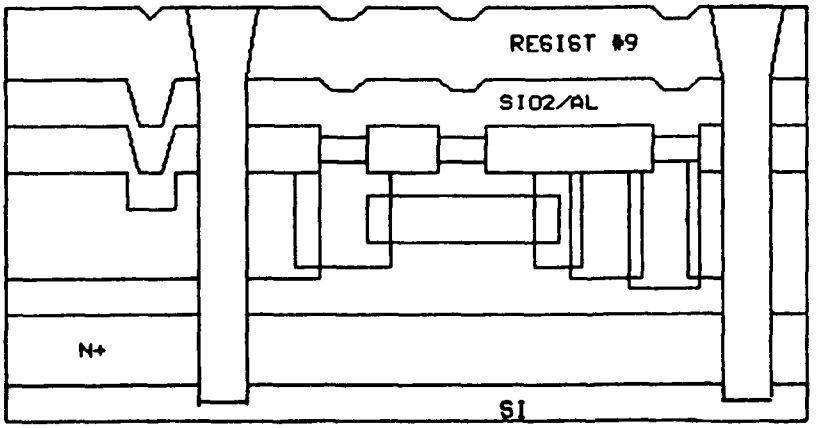
Figure 3(b).



DEPOSIT 3000A° NITRIDE
PATTERN N-CONTACTS
ETCH NITRIDE
DEPOSIT N-OHMIC METAL
LIFT-OFF N-OHMIC METAL AND STRIP RESIST



COAT WITH RESIST
PATTERN P-CONTACTS
ETCH NITRIDE
DEPOSIT P-OHMIC METAL
STRIP RESIST AND LIFT-OFF METAL



DEPOSIT 500 SIO2
DEPOSIT 3000A° AL
PATTERN TRENCH
ETCH AL
ETCH SIO2/SI3N4
ETCH GAAS TRENCH
STRIP RESIST
DEPOSIT NITRIDE
PLANARIZE SURFACE
STRIP AL

(NOT SHOWN)
PATTERN & ETCH VIAS
DEPOSIT METAL
PATTERN & ETCH METAL

Figure 3(c).

increase the f_t. In addition, a self-aligned transistor process will also be developed to improve speed. The overgrowth process can be used with both the baseline (nonself-aligned) process as well as with the advanced self-aligned HBT process.

C. Overgrowth Epitaxial Process

In the conventional mesa HBT, the base is doped as the epitaxial layer is grown and the maximum base doping concentration is limited primarily by the necessity for high current gain and, to a lesser extent, by the solubility limit. For the planar baseline process outlined in Figure 3, the base is implanted selectively into the substrate. The base implant dose is limited by the requirement that the tail of the implant distribution not compensate the donors in the emitter region adjacent to the AlGaAs-GaAs interface. This places an upper limit on the magnitude of the base dose and therefore a lower limit on the base resistance.

To lower the base resistance and increase the f_t, it is necessary to increase the base doping concentration beyond that of the HBT emitter. To accomplish this while still maintaining the planar structure (nonmesa), an overgrowth process is being developed. For this overgrowth process, the base is implanted into the GaAs prior to the deposition of the final AlGaAs emitter layer.

In the overgrowth process, a sacrificial layer such as epitaxial $Al_{0.5}Ga_{0.5}As$ or nitride will be deposited over the GaAs base area to act as a spacer for the base implant. To maximize the electric field in the base such that the electron transit time is minimum, the peak in the base doping concentration should occur at the emitter-base junction. The spacer thickness is adjusted such that the peak of the implant occurs at the spacer-GaAs interface. The high (50%) aluminum concentration in the AlGaAs spacer layer permits its easy removal from the underlying GaAs surface after the activation anneal of the base implant. After the removal of the spacer layer, the hetero-epitaxial $Al_{0.3}Ga_{0.7}As$ emitter and GaAs cap layers are grown on the substrate.

The first lot of the overgrowth material has been started using an existing mask set based on the HI^2L transistor structure. The advantages to using the HI^2L mask set are simplicity and a fast lot start. The initial spacer layer being examined is the $Al_{0.5}Ga_{0.5}As$ epi layer on top of the base and emitter regions (emitter down HI^2L), which acts both as a spacer and as a cap layer for the implant activation anneal. This lot has been successfully processed through the removal of the $Al_{0.5}Ga_{0.5}As$ epi layer, deposition of the overgrowth epi layers, and is nearing the point in the process where the transistors can be hand-probed prior to deposition of the first level metal leads.

D. Self-Aligned HBT Structures

The self-aligned HBT process has been outlined in our original proposal and is similar to TI's self-aligned MESFET process. Due to our emphasis on understanding the interrelationships between the various fundamental process steps and the transistor dc performance, the baseline process will be developed initially since it is somewhat simpler. Parameters affecting the dc performance for the baseline process and the self-aligned process are expected to be the same. The self-aligned HBT process is scheduled to begin development during the last half of this contract year and will draw heavily from our efforts on the nonself-aligned process as well as from our on-going MESFET programs.

E. Heterojunction Material Evaluation

As stated above, the initial process development will concentrate on the base implanted through the emitter layer technique. This technique has proven successful in the past and is the starting point for this contract. The initial process development will primarily use MOCVD-grown structures, which is an advantage since each MOCVD batch has five wafers. We will reserve one wafer from each batch to do an extensive materials analysis, including capacitance-voltage, photoluminescence, and secondary ion mass spectroscopy. This material analysis can be correlated later with the transistor results obtained from the remaining four wafers in each MOCVD batch.

The epitaxial structures ordered for the initial process development are presented in Table 3. The constants in the epi structures are a 200 Å graded Al layer between the cap layer and the emitter, the 10,000 Å subcollector, and the n^+ GaAs Bridgman substrate. The n^+ substrate precludes the fabrication of circuits; however, it simplifies the analysis of the transistors and reduces the cycle time. Once an epi-structure has been optimized, it will then be grown on semi-insulating GaAs. The wafers will be processed with different base fluence and energies so that the optimum base width and doping can be found. The first pass Be base implantation experiments are presented in Table 4. An example of the concentration vs depth profile for a typical epi structure and base implantation variation within the E-series of lots 6 through 9 is shown in Figure 4. The impact of these base profiles on the transistor gains, base sheet resistance, leakage currents, and breakdown voltages will be evaluated using these and similar process splits.

The variations in the epi layers, Table 3, will also be used to examine trade-offs between reduced contact resistance, base sheet resistance, V_{be} uniformity, and gain. The thick cap layer epis (lots 1 through 6) are expected to have lower contact resistance than the thin cap layer structures (lots 7 through 9). However, this is a trade-off with the base thickness and concentration because the base must be implanted through the cap and emitter layer. Additionally, the thick cap layer structures are desirable for fabricating JFETs in the cap layer. The heterojunction interface will be examined by grading the Al over 300 Å or 600 Å (lot 4), by grading n-type doping in the Al graded region (lots 5,9) and by grading the Al throughout the base region (lot 6). Additionally, the use of an undoped spacer layer between the emitter and the base region will be examined (lots 2,8). The first four of these epi lots have been received and the HBT processing using the new mask set has begun.

The overgrowth technique will be approached carefully. The two MOCVD epitaxial structures that will be examined first use a different method of base tailoring, Table 5. Lot 1 uses a sacrificial AlGaAs layer while the second lot will use a layer of silicon nitride as the sacrificial layer for removing the first half of the Be base implant profile. The second epi will

Table 3. Epitaxial Structures Ordered for the Initial Process Development

Lot	layer thickness (Å) Concentration (/cm^3)			Al->	n->	Coll	sub-C	Substrate
	cap	Al<-	emit					
THICK CAP LAYER								
1	1200 2 x 10^{18}	200 2 x 10^{18}	1000 2 x 10^{18}	300 2 x 10^{18}	--- ---	5000 5 x 10^{16}	10,000 2 x 10^{18}	Bridgman 1 x 10^{18}
2	1200 2 x 10^{18}	200 2 x 10^{18}	1000 2 x 10^{18}	300 2 x 10^{18}	100 < 1 x 10^{15}	5000 5 x 10^{16}	10,000 2 x 10^{18}	Bridgman 1 x 10^{18}
3	1200 2 x 10^{18}	200 2 x 10^{18}	1600 2 x 10^{18}	300 2 x 10^{18}	--- ---	5000 5 x 10^{16}	10,000 2 x 10^{18}	Bridgman 1 x 10^{18}
4	1200 2 x 10^{18}	200 2 x 10^{18}	1300 2 x 10^{18}	600 2 x 10^{18}	--- ---	5000 5 x 10^{16}	10,000 2 x 10^{18}	Bridgman 1 x 10^{18}
5	1200 2 x 10^{18}	200 2 x 10^{18}	1000 2 x 10^{18}	300 2 x 10^{18}	< (300) <------	5000 5 x 10^{16}	10,000 2 x 10^{18}	Bridgman 1 x 10^{18}
6	1200 2 x 10^{18}	200 2 x 10^{18}	1000 2 x 10^{18}	300 2 x 10^{18}	+1500 5 x 10^{16}	3500 5 x 10^{16}	10,000 2 x 10^{18}	Bridgman 1 x 10^{18}
THIN CAP LAYER								
7	500 2 x 10^{18}	200 2 x 10^{18}	1700 2 x 10^{18}	300 2 x 10^{18}	--- ---	5000 5 x 10^{16}	10,000 2 x 10^{18}	Bridgman 1 x 10^{18}
8	500 2 x 10^{18}	200 2 x 10^{18}	1700 2 x 10^{18}	300 2 x 10^{18}	100 < 1 x 10^{15}	5000 5 x 10^{16}	10,000 2 x 10^{18}	Bridgman 1 x 10^{18}
9	500 2 x 10^{18}	200 2 x 10^{18}	1700 2 x 10^{18}	300 2 x 10^{18}	< (300) <------	5000 5 x 10^{16}	10,000 2 x 10^{18}	Bridgman 1 x 10^{18}

Table 4. Be Base Implantation Matrix

MOCVD*	A	B	C	E**
#1	Con	+2	-1	+1
#2	+2	Con	-2	-2
#5	+3	+1	Con	-3
#6	-1	-3	+3	Con
#7	Con	+2	-1	+1
#8	+2	Con	-2	-2
#9	-1	+1	Con	-3
#3	Con	+1	+2	+3
#4	+3	Con	+1	+2

Key Symbol	Energy keV	Fluence $1 \times 10^{13}/cm^2$
Con	= 70	2
+1	90	2
+2	70	4
+3	90	4
-1	50	2
-2	70	1
-3	50	1

* Note: The total cap and emitter thickness of MOCVD #3 and #4 is 3300 Å, while the rest of the lots are 2700 Å.

** Note: The five wafers from each MOCVD batch are labeled A, B, C, D, E. Wafer D will be used for materials analysis.

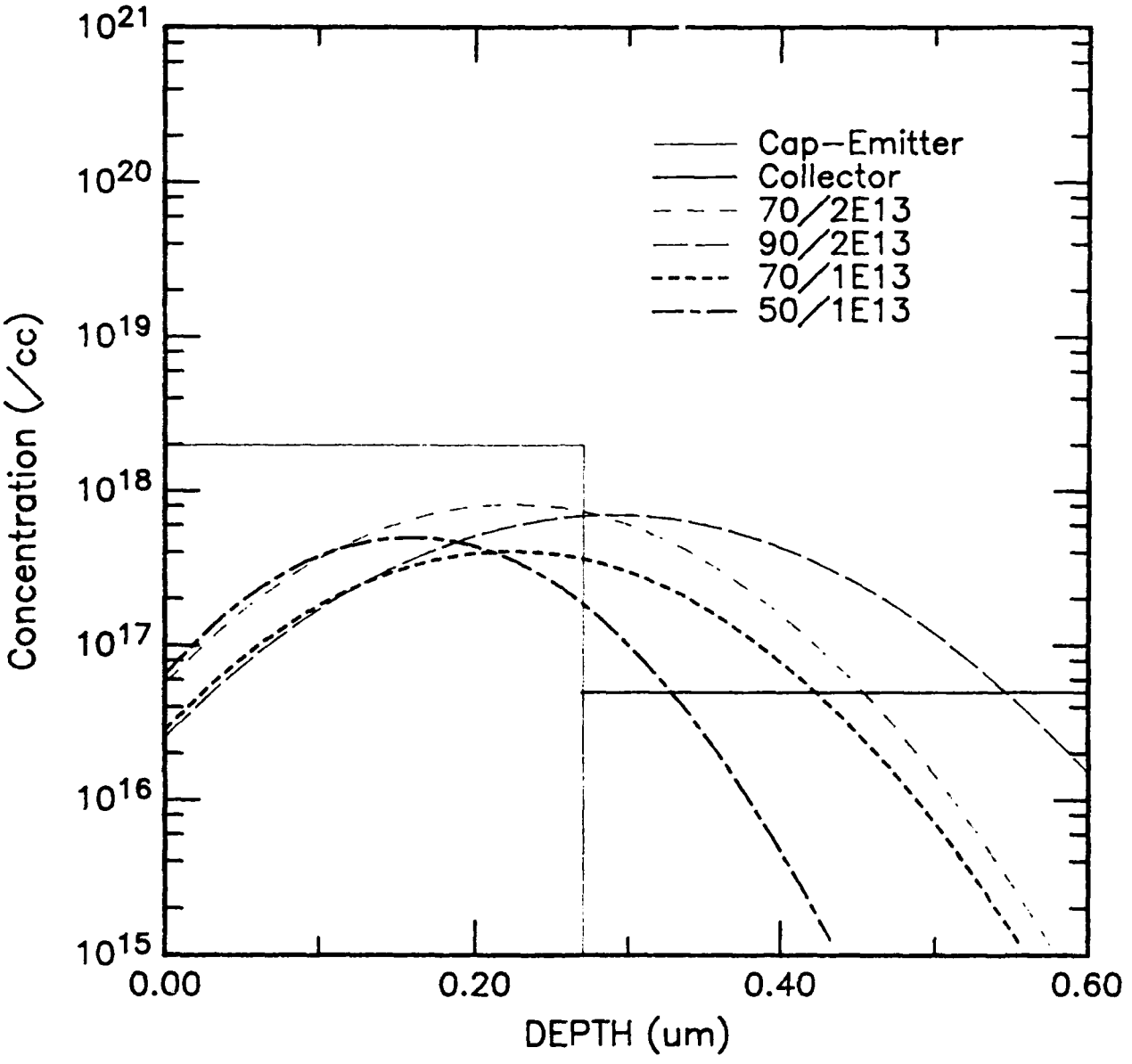


Figure 4. Be base implantation, E series Lot #6-9.

Table 5. Base Tailoring for MOCVD Epitaxial Structures

FIRST EPI FOR OVERGROWTH								
Lot	layer thickness (Å) Concentration ($/cm^3$)			Al->	n->	Coll	sub-C	Substrate
	cap	Al<-	emit					
1	1000 UNDOPED	(0.5 AlAs) UNDOPED	--- ---	--- ---	--- ---	5000 5×10^{16}	10,000 2×10^{18}	Bridgman 1×10^{18}
2	--- ---	--- ---	--- ---	--- ---	--- ---	5000 5×10^{16}	10,000 2×10^{18}	Bridgman 1×10^{18}

SECOND OVERGROWTH EPI

1	1200 2×10^{18}	200 2×10^{18}	1000 2×10^{18}	300 2×10^{18}	--- ---			
2	1200 2×10^{18}	200 2×10^{18}	1000 2×10^{18}	300 2×10^{18}	100 $< 1 \times 10^{15}$			

be done on two wafers at a time, one from each batch of the first epi, using different precleaning techniques and anneals until an optimum procedure is obtained.

III. ANALOG-TO-DIGITAL CONVERTER DESIGN

During the first quarter only minimal effort was directed at the ADC circuit design due to not having Hughes under contract. Hughes began working on this program at the beginning of July and the first joint meeting between Hughes and TI to discuss the technical aspects of the program is schedule for 29 July 1987.

W. R. WISSEMAN, Program Manager
System Components Laboratory